REMARKS

Claims 1-14, 16-21, 23-28 and 31-40 are pending. Claims 1-14, 16-21 and 34-40 are allowed. Claims 23, 25, 27 and 32 have been amended. In view of the following, all pending claims are in condition for allowance. **But if after considering this response the Examiner does not agree that all of the claims are in condition for allowance, then the Examiner is requested to schedule an interview with the Applicants' attorney to further prosecution of this application.**

Rejection of Claims 23-28 and 31-33 Under 35 U.S.C. § 112, second paragraph

Claims 23 and 27 have been amended to overcome this rejection. Claims 25 and 32 have been amended to correct antecedent basis.

Rejection of Claims 23-26 Under 35 U.S.C. § 102(b) As Being Anticipated by Biggs et al. (US 6,128,716)

Claim 23

Claim 23, as amended, recites receiving an address strobe at a first node of a first portion of a memory circuit, receiving a first address at a second node of the first portion of the memory circuit, generating a second address within the first portion of the memory circuit, and comparing the first address to the second address within the first portion of the memory circuit.

For example, referring to FIGS. 4-5 and pages 6-11 of the present application, an address strobe (CAS) is received at a first node (CAS) of a first portion (12) of a memory circuit (26), a first address (ADDRESS) is received at a second node (ADDRESS) of the first portion (12) of the memory circuit (26), a second address (INTERNAL COLUMN ADDRESS) is generated within the first portion (12, and more specifically 14) of the memory circuit (26), and the first address (ADDRESS) is compared to the second address (INTERNAL COLUMN ADDRESS) within the first portion (12, and more specifically 18) of the memory circuit (26). It should be noted that this all occurs within the first portion (12) of the

memory circuit (26), and that the first portion (12) receives the address strobe (CAS).

In contrast, Biggs does not disclose receiving an address strobe at a first node of a first portion of a memory circuit, receiving a first address at a second node of the first portion of the memory circuit, generating a second address within the first portion of the memory circuit, and comparing the first address to the second address within the first portion of the memory circuit. Instead, Biggs simply discloses a first portion 43 of a memory circuit that receives an address strobe CAS from a memory controller 42 (FIG. 1). The DRAM 43 is the only portion of the memory circuit in Biggs that receives any kind of address strobe. However, the DRAM 43 is simply a memory array and is unable to generate an address or compare two addresses. In fact, the only portions of the memory circuit in Biggs that are capable of generating an address or comparing two addresses are located within the memory controller 42 (FIG. 1). The memory controller 42 is entirely separate from the DRAM 43, and does not receive any address strobe whatsoever. To the contrary, the memory controller 42 actually generates the address strobe CAS instead of receiving it.

The Examiner states on page 4 of the Office Action that she considers the combination of memory controller 42 and memory 43 to be the entire memory circuit. However, claim 23 has been amended to recite that only a first portion of the memory circuit receives the address strobe, and that within this first portion the second address must be generated and the first and second address must be compared. Because only the DRAM 43 receives the address strobe CAS in Biggs, the DRAM 43 must be considered the "first portion of the memory circuit." However, as discussed above, the DRAM 43 is unable to generate an address or compare two addresses. The Examiner even concedes on page 4 of the Office Action that she considers the "first address" to be R2C2, the "second address" to be R3C3, and quotes col. 4, lines 57-67 of Biggs to describe her reasoning. However, the generating and comparing of R2C2 and R3C3 are both performed entirely by memory controller 42 (col. 4, lines 57-67). As discussed above, the memory controller 42 cannot be considered the "first portion of the memory circuit" because the memory controller 42 does not receive the address strobe CAS (only the DRAM 43 receives the address strobe CAS).

Therefore, Biggs does not satisfy the limitations of amended claim 23.

Claims 24-26

Claims 24-26 are patentable by virtue of their dependency from independent claim 23.

Rejection of Claims 27-28 and 31-33 Under 35 U.S.C. § 102(b) As Being Anticipated by Ryan et al. (US 5,966,724)

Claim 27

Claim 27, as amended, recites loading a memory circuit with a predetermined value; receiving a first address at a first node of the memory circuit during a data transfer cycle, the first address generated from a source external to the memory circuit; comparing the first address to the predetermined value within the memory circuit; and terminating the data-transfer cycle if the first address has a predetermined relationship to the predetermined value.

For example, referring to FIGS. 4-5 and pages 6-11 of the patent application, a memory circuit (26) is loaded with a predetermined value (in register/counter 16); a first address is received at a first node (ADDRESS) of the memory circuit (26); the first address and the predetermined value are compared within the memory circuit (26, and more specifically, 18); and the data-transfer cycle is terminated (by control circuit 24) if the first address has a predetermined relationship (*e.g.*, is equal) to the predetermined value (in register/counter 16). It should be noted that this all occurs within the memory circuit (26), and that the first address (ADDRESS) is generated from a source external to the memory circuit (26).

In contrast, Ryan does not disclose loading a memory circuit with a predetermined value; receiving a first address at a first node of the memory circuit during a data transfer cycle, the first address generated from a source external to the memory circuit; comparing the first address to the predetermined value within the memory circuit; and terminating the data-transfer cycle if the first address has a predetermined relationship to the predetermined value. Instead, Ryan simply discloses a control circuitry 38 that contains an initial address latch and a

comparator that compares the initial address (predetermined value) with "internally generated addresses" and terminates the burst access when a match occurs (FIG. 1; col. 5, lines 49-54). However, this is contrary to the limitations of claim 27 because the control circuitry 38 compares the initial address (predetermined value) to an address that is "internally generated" instead of an address that is generated from a source external to the control circuitry 38. Even if the Examiner were to argue that the memory circuit is restricted to memory array 12 so that the addresses generated by the control circuitry 38 are external to the memory array 12, then the limitations of claim 27 are still not satisfied because the memory array 12 is itself unable to compare an address to a predetermined value. Therefore, Ryan does not satisfy the limitations of claim 27.

Claims 28-33

Claims 28-33 are patentable by virtue of their dependency from independent claim 27.

CONCLUSION

In light of the foregoing, all pending claims are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 08-2025.

If after considering this response the Examiner does not agree that all pending claims are in condition for allowance, the Examiner is requested to schedule an interview with the Applicants' attorney at (425) 455-5575 to further prosecution of this application.

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Respectfully Submitted,

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